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Analysis of a 2 ×/ 1.5 ×/ 1 × Mode DC-DC Converter Designed by Using Switched-Capacitor Techniques

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Abstract: For mobile applications, a switched-capacitor (SC) DC-DC converter which offers a 2 ×/ 1.5 ×/ 1 × mode of operation is presented, and its properties are analyzed theoretically in this paper. Aimed at backlighting applications, battery applications, etc., the proposed converter provides stepped-up/stepped-down voltages. Compared with the conventional approaches employing doubler circuits, the proposed converter can realize high efficiency and flexibility of output voltages. The validity of the proposed converter is confirmed by SPICE simulations and theoretical analyses. Concerning the power efficiency and the optimal duty factor, the confirmation result shows that the theoretical results correspond to the simulation results well. Furthermore, under the conditions that the input voltage V_{in} =3.7 V, the output load $R_L = 30\,\Omega$, and the output voltage $V_{out} = 3.3 \sim 5.3$ V, the proposed converter can improve the power efficiency more than twice from that of the conventional circuit.

Keywords: DC-DC converters; Switched-capacitor circuits; Backlighting applications; Versatile converters; Discrete-time circuits

1. Introduction

Recently, according to the down-scaling of portable electronic products, power converters designed by using switched-capacitor (SC) techniques [1-16] attract much attention. Since no magnetic elements are required to design the SC power converters, they can realize thin circuit composition, light-weight and low-noise. For this reason, the SC power converter is used as a driver circuit of white LEDs for display backlighting, a building block of battery management systems, and so on. For example, in mobile backlighting applications, the stepped-up voltage such as $4.75 \sim 6.5$ V (Typ. = 5 V) is required to drive some LEDs at up to 25 mA. On the other hand, to extend the battery life, versatile SC converters which can provide step-up/step-down voltages are necessary.

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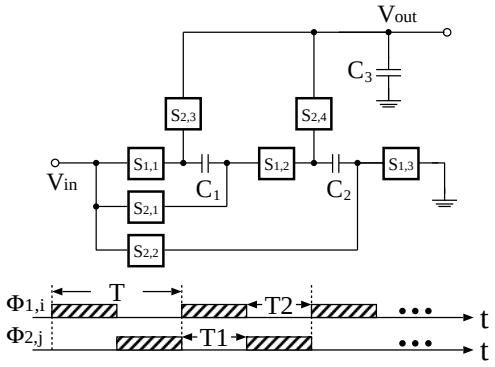


Figure 1. Proposed SC DC-DC converter.

To adjust the output voltage, on-resistance control scheme [9,12,13,16] or pulse width modulation (PWM) scheme [10, 11] is usually employed in the SC DC-DC converter, because the ratio of the voltage conversion is predetermined by circuit structure. The power efficiency of the SC power converters gets worse by the regulation of the output voltage. In the case of a voltage doubler circuit [14-16], for example, the efficiency decreases greatly when the low output voltage is required, because the output voltage must be regulated strongly. To solve this problem, we proposed the circuit topology of a 1.5 $\times$ mode SC DC-DC converter in [9], because it is necessary to create a 5 V power supply [1] from a 3.7 V supply of a lithium-ion battery. However, by changing the control scheme of clock pulses, fortunately, the converter proposed in [9] can work as a versatile step-up/step-down converter which can offer a 2 $\times$/ 1.5 $\times$/ 1 $\times$ mode of operation. As mentioned above, to extend the battery life, the step-up/step-down converters are useful.

In this paper, aimed at backlighting applications, battery management applications, etc., the converter proposed in [9] is modified to provide stepped-up / stepped-down voltages, and the handy theoretical formulas are given concerning the power efficiency and the optimal duty factor. Compared with the conventional versatile converters based on doubler circuits [16], the proposed converter can realize high efficiency and flexibility of output voltages, because it offers a 2 $\times$/ 1.5 $\times$/ 1 $\times$ mode of operation. To confirm the validity of the circuit design and the theoretical analyses, SPICE simulations are performed.

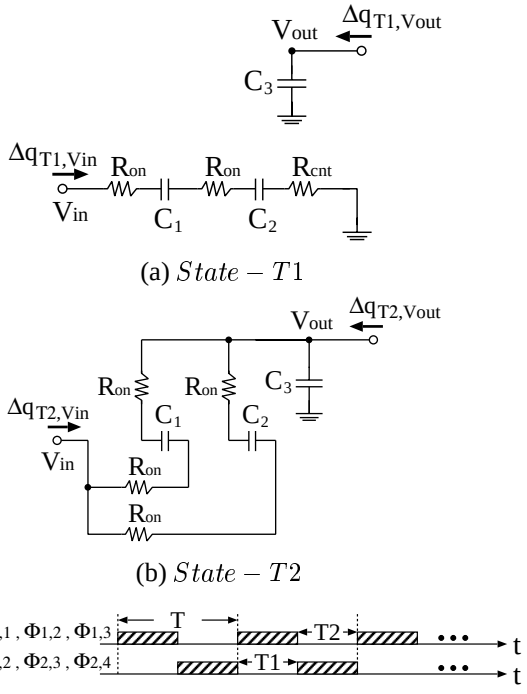


Figure 2. Instantaneous equivalent circuits when 1.5 $\times$ mode of operation.

2. Circuit Structure

Figure 1 shows a 1.5 $\times$ mode DC-DC converter designed by using the SC technique [9]. The converter consists of 7 power switches and 3 capacitors. In Fig.1, the power switches $S_{1,i}$ and $S_{2,j}$ $((i = 1, \ldots, 3)$ and $(j = 1, \ldots, 4))$ are driven by 2-phase clock pulses $\Phi_{1,i}$ and $\Phi_{2,j}$, respectively. The interval of $\Phi_{1,i}$ and $\Phi_{2,j}$ is set to as follows:

$$\begin{aligned} T &= T1 + T2, \\ T1 &= DT, \\ \text{and} \quad T2 &= (1-D)T, \end{aligned} \tag{1}$$

where T is a period of the clock pulse and D denotes a duty factor. By controlling the power switches $S_{1,i}$ and $S_{2,j}$, the converter performs a DC-DC conversion.

The control scheme and the circuit properties for a 2 $\times$/ 1.5 $\times$/ 1 $\times$ conversion will be described in the following section.

3. Theoretical Analysis

3.1 1.5 $\times$ Mode

First, the equivalent circuit when a 1.5 $\times$ mode is analyzed. In the theoretical analysis, we assume that

[1] The typical voltage for backlighting applications is 5 V.

1. parasitic elements are not effective and 2. the time constant is quite larger than a period of the clock pulse.

Figure 2 shows the instantaneous equivalent circuits in the case of the 1.5 $\times$ mode. In the steady state, the differential values of the electric charges in C_k^i $(k = 1, 2, 3)$ satisfy

$$\Delta q_{T1}^k + \Delta q_{T2}^k = 0, \quad (2)$$

where Δq_{T1}^k and Δq_{T2}^k denote the electric charges when $State - T1$ and $State - T2$, respectively. In the case of $State - T1$, the differential values of the electric charges in the input and the output terminals, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$, are given by

$$\begin{aligned} &\Delta q_{T1,V_{in}} = \Delta q_{T1}^1 = \Delta q_{T1}^2 \\ \text{and} \quad &\Delta q_{T1,V_{out}} = \Delta q_{T1}^3. \end{aligned} \quad (3)$$

On the other hand, in the case of $State - T2$, the differential values of the electric charges in the input and the output terminals, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$, are given by

$$\begin{aligned} &\Delta q_{T2,V_{in}} = -(\Delta q_{T2}^1 + \Delta q_{T2}^2) \\ \text{and} \quad &\Delta q_{T2,V_{out}} = \Delta q_{T2}^1 + \Delta q_{T2}^2 + \Delta q_{T2}^3. \end{aligned} \quad (4)$$

Here, the average currents of the input and the output are given by

$$\begin{aligned} \overline{I_{in}} &= (\Delta q_{T1,V_{in}} + \Delta q_{T2,V_{in}})/T \\ &= \Delta q_{V_{in}}/T \\ \text{and} \quad \overline{I_{out}} &= (\Delta q_{T1,V_{out}} + \Delta q_{T2,V_{out}})/T \\ &= \Delta q_{V_{out}}/T, \end{aligned} \quad (5)$$

where $\Delta q_{V_{in}}$ and $\Delta q_{V_{out}}$ are the electric charges in the input and the output, respectively. From Eqs.(2) $\sim$ (5), the following equation is derived:

$$\overline{I_{in}} = -\frac{3}{2}\overline{I_{out}}. \quad (6)$$

In Fig.2, the energy consumed by resistors in one period, W_T, can be expressed by

$$W_T = W_{T1} + W_{T2}, \quad (7)$$

where

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{T1}(\Delta q_{T1}^1)^2 + \frac{R_{cnt}}{T1}(\Delta q_{T1}^1)^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{T2}(\Delta q_{T2}^1)^2 + \frac{2R_{on}}{T2}(\Delta q_{T2}^2)^2. \end{aligned}$$

From Eqs.(1) $\sim$ (5), Eq.(7) can be rewritten as

$$\begin{aligned} W_{T1} &= \frac{R_{on}}{2DT}(\Delta q_{V_{out}})^2 + \frac{R_{cnt}}{4DT}(\Delta q_{V_{out}})^2 \\ \text{and} \quad W_{T2} &= \frac{R_{on}}{(1-D)T}(\Delta q_{V_{out}})^2. \end{aligned} \quad (8)$$

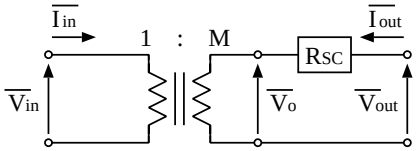


Figure 3. General form of equivalent circuit.

Here, a general equivalent circuit of SC power converters [3,4,9,12] can be given by the circuit shown in Fig.3, where R_{SC} is called an SC resistance, M is a ratio of the ideal transformer, and $\overline{V_{in}}$ and $\overline{V_{out}}$ denote an averaged input voltage and an averaged output voltage, respectively. The consumed energy W_T of Fig.3 can be expressed by

$$\begin{aligned} W_T &= W_{T1} + W_{T2} \\ &= (\frac{\Delta q_{V_{out}}}{T})^2 \cdot R_{SC} \cdot T. \end{aligned} \quad (9)$$

By substituting Eq.(8) into Eq.(9), the SC resistance when the 1.5 $\times$ mode, $R_{SC,3/2}$, is given by

$$\begin{aligned} R_{SC,3/2} &= \frac{2(1+D)}{4D(1-D)} \cdot R_{on} \\ &\quad + \frac{1-D}{4D(1-D)} \cdot R_{cnt}. \end{aligned} \quad (10)$$

The equivalent circuit of Fig.3 can be expressed by the determinant using a Kettenmatrix. Therefore, by using Eqs.(6) and (10), the equivalent circuit of the proposed converter is given by the following determinant:

$$\begin{aligned} &\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \\ &\begin{bmatrix} \frac{2}{3} & 0 \\ 0 & \frac{3}{2} \end{bmatrix} \begin{bmatrix} 1 & R_{SC,3/2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \end{aligned} \quad (11)$$

As Eq.(11) shows, the output voltage of the proposed circuit becomes $(3/2)V_{in}$ when $R_{SC,3/2} \ll R_L$.

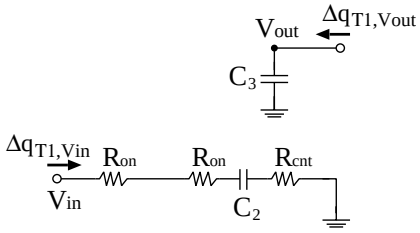
From Eq.(11), the averaged output voltage $\overline{V_{out}}$ is expressed by

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC,3/2}} \cdot (\frac{3}{2}\overline{V_{in}}). \quad (12)$$

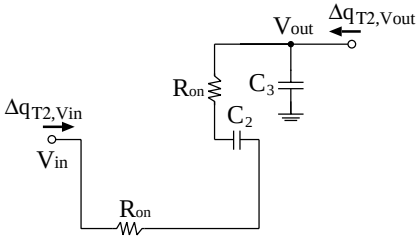
Furthermore, the power efficiency $\eta_{3/2}$ [2] can be given by

$$\eta_{3/2} = \frac{R_L \overline{I_{out}}^2}{R_L \overline{I_{out}}^2 + R_{SC,3/2}\overline{I_{out}}^2}$$

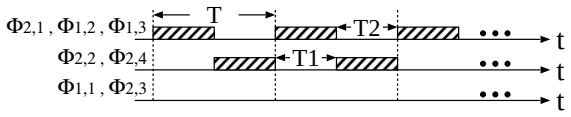
[2] Of course, the consumed energy of the peripheral circuits such as pulse generators, comparators, etc. is disregarded in the power efficiency of Eq.(13).



(a) $State - T1$



(b) $State - T2$



(c) Timing of pulses

Figure 4. Instantaneous equivalent circuits when 2 $\times$ mode of operation.

$$= \frac{R_L}{R_L + R_{SC,3/2}}. \qquad (13)$$

where $R_{SC,3/2}$ depends on the resistance R_{cnt} shown in Eq.(10). As Eq.(13) shows, $\overline{V_{out}}$ can be regulated by controlling R_{cnt} which corresponds to the on-resistance of $S_{1,3}$ (see in Fig.2.). In other word, the regulation is achieved by controlling the gate voltage of $S_{1,3}$.

As Eq.(13) shows, the increase of the $R_{SC,3/2}$ causes the decrease of the efficiency $\eta_{3/2}$. In other word, the maximum power efficiency is obtained when $R_{cnt} = R_{on}$. From Eq.(10), the minimum on-resistance $\min(R_{SC,3/2})$ can be expressed by

$$\min(R_{SC,3/2}) = \frac{(D+3)}{4D(1-D)} \cdot R_{on}. \qquad (14)$$

In Eq.(14), the optimum value of the parameter D is obtained when

$$\frac{d\min(R_{SC,3/2})}{dD} = 0 \quad \text{and} \quad 0 < D < 1. \qquad (15)$$

From Eqs.(14) and (15), the optimal duty factor for the 1.5 $\times$ mode is $D \simeq 0.46$ [3] .

[3] In other word, the power efficiency becomes the maximum value when $D \simeq 0.46$.

3.2 2 $\times$ Mode

Figure 4 shows the instantaneous equivalent circuits in the case of a 2 $\times$ mode. In Fig.4 (a), the differential values of the electric charges, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$, are given by

$$\begin{aligned} & \Delta q_{T1,V_{in}} = \Delta q_{T1}^2 \\ \text{and} \quad & \Delta q_{T1,V_{out}} = \Delta q_{T1}^3. \end{aligned} \qquad (16)$$

In Fig.4 (b), the differential values of the electric charges, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$, are given by

$$\begin{aligned} & -\Delta q_{T2,V_{in}} = \Delta q_{T2}^2 \\ \text{and} \quad & \Delta q_{T2,V_{out}} = \Delta q_{T2}^2 + \Delta q_{T2}^3. \end{aligned} \qquad (17)$$

From Eqs.(2), (5), (16), and (17), the relation between the input current and the output current is derived as

$$\overline{I_{in}} = -2\overline{I_{out}}. \qquad (18)$$

In Figs.4 (a) and (b), the energy consumed by resistors in one period, W_{T1} and W_{T2}, can be expressed by

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{T1}(\Delta q_{T1}^2)^2 + \frac{R_{cnt}}{T1}(\Delta q_{T1}^2)^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{T2}(\Delta q_{T2}^2)^2, \end{aligned} \qquad (19)$$

respectively. From Eqs.(1), (2), (5), (16), and (17), Eq.(19) can be rewritten as

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{DT}(\Delta q_{V_{out}})^2 + \frac{R_{cnt}}{DT}(\Delta q_{V_{out}})^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{(1-D)T}(\Delta q_{V_{out}})^2. \end{aligned} \qquad (20)$$

By substituting Eq.(20) into Eq.(9), the SC resistance for the 2 $\times$ mode, $R_{SC,2}$, can be expressed by

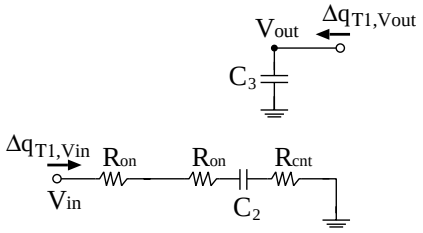
$$R_{SC,2} = \frac{2}{D(1-D)} \cdot R_{on} + \frac{1}{D} \cdot R_{cnt}. \qquad (21)$$

Therefore, by using Eqs.(18) and (21), the equivalent circuit is given by the following determinant:

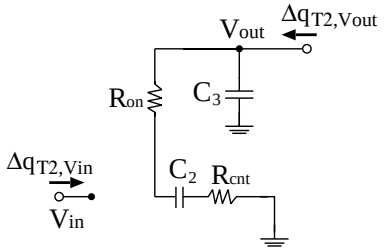
$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & 0 \\ 0 & 2 \end{bmatrix} \begin{bmatrix} 1 & R_{SC,2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \qquad (22)$$

From Eq.(22), the averaged output voltage $\overline{V_{out}}$ is expressed by

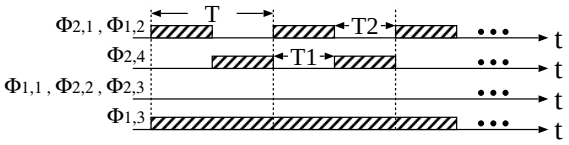
$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC,2}} \cdot (2\overline{V_{in}}). \qquad (23)$$



(a) $State - T1$



(b) $State - T2$



(c) Timing of pulses

Figure 5. Instantaneous equivalent circuits when 1 $\times$ mode of operation.

Furthermore, the power efficiency η_2 can be given by

$$\begin{aligned}\eta_2 &= \frac{R_L\overline{I_{out}}^2}{R_L\overline{I_{out}}^2 + R_{SC,2}\overline{I_{out}}^2} \\ &= \frac{R_L}{R_L + R_{SC,2}}. \end{aligned} \quad (24)$$

As Eqs.(21) and (23) show, $\overline{V_{out}}$ can be regulated by controlling R_{cnt} (see in Fig.3.). From Eqs.(21) and (24), the maximum efficiency is obtained under the condition that

$$R_{SC,2} = \frac{2}{D(1-D)} \cdot R_{on} + \frac{1}{D} \cdot R_{on}, \quad (25)$$

because the minimum on-resistance $\min\{R_{SC,2}\}$ is obtained when $R_{cnt} = R_{on}$. From Eqs.(25), the optimal duty factor is $D \simeq 0.55$.

3.3 1 $\times$ Mode

Figure 5 shows the instantaneous equivalent circuits in the case of a 1 $\times$ mode. In Fig.5 (a), the differential values of the electric charges, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$, are given by

$$\begin{aligned} &\Delta q_{T1,V_{in}} = \Delta q_{T1}^2 \\ \text{and} \quad &\Delta q_{T1,V_{out}} = \Delta q_{T1}^3. \end{aligned} \quad (26)$$

In Fig.5 (b), the differential values of the electric charges, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$, are given by

$$\begin{aligned} &\Delta q_{T2,V_{in}} = 0 \\ \text{and} \quad &\Delta q_{T2,V_{out}} = \Delta q_{T2}^2 + \Delta q_{T2}^3. \end{aligned} \quad (27)$$

From Eqs.(2), (5), (26), and (27), the relation between the input current and the output current is derived as

$$\overline{I_{in}} = -\overline{I_{out}}. \quad (28)$$

In Figs.5 (a) and (b), W_{T1} and W_{T2} can be expressed by

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{T1}(\Delta q_{T1}^2)^2 + \frac{R_{cnt}}{T1}(\Delta q_{T1}^2)^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{T2}(\Delta q_{T2}^2)^2, \end{aligned} \quad (29)$$

respectively. As Eqs.(19) and (29) show, the consumed energy W_{T1} and W_{T2} for the case of the 2 $\times$ mode is equal to that for the case of the 1 $\times$ mode. Therefore, the SC resistance for the 1 $\times$ mode, $R_{SC,1}$, can be expressed by

$$R_{SC,1} = \frac{2}{D(1-D)} \cdot R_{on} + \frac{1}{D} \cdot R_{cnt}. \quad (30)$$

Therefore, by using Eqs.(28) and (30), the equivalent circuit can be given by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_{SC,1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \quad (31)$$

As Eq.(31) shows, the output voltage of the proposed circuit becomes V_{in} when $R_{SC,1} \ll R_L$.

From Eq.(31), the averaged output voltage $\overline{V_{out}}$ is expressed by

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC,1}} \cdot \overline{V_{in}}. \quad (32)$$

As Eqs.(30) and (32) show, the step-down conversion can be achieved by controlling R_{cnt} (see in Fig.5.). Therefore, different from [16], the proposed converter can regulate the output voltage in not only the step-up case but also the step-down case.

From Eq.(31), the power efficiency η_1 can be given by

$$\begin{aligned}\eta_1 &= \frac{R_L\overline{I_{out}}^2}{R_L\overline{I_{out}}^2 + R_{SC,1}\overline{I_{out}}^2} \\ &= \frac{R_L}{R_L + R_{SC,1}}. \end{aligned} \quad (33)$$

From Eqs.(30) and (33), the maximum efficiency is obtained when $D \simeq 0.55$, because Eq.(30) is equal to Eq.(21).

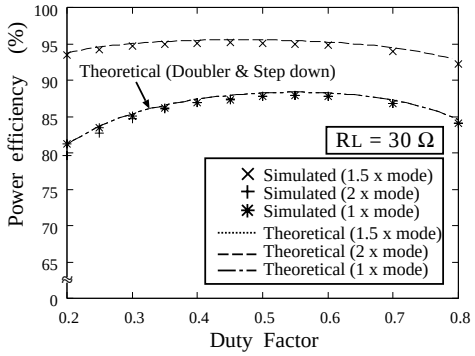


Figure 6. Power efficiency as function of parameter D.

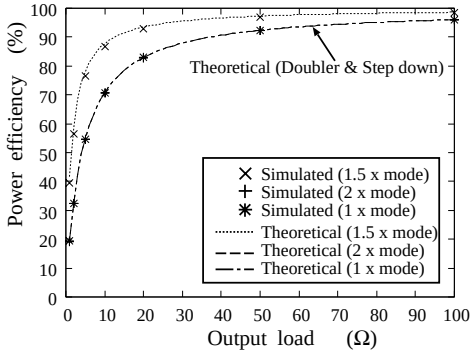


Figure 8. Power efficiency as function of output load R_L.

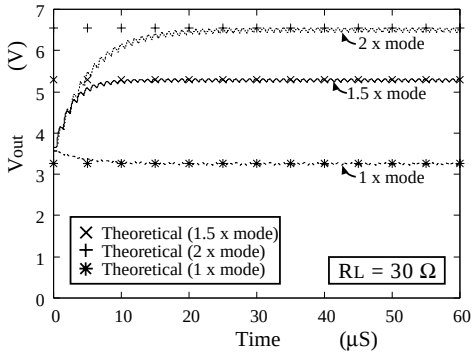


Figure 7. Output voltage with different conversion ratios.

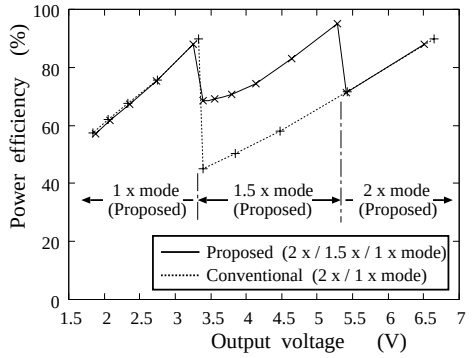


Figure 9. Power efficiency as function of output voltage V_{out}.

4. Simulation

To confirm the validity of the circuit design and the theoretical analyses, SPICE simulations were performed under the conditions that the input voltage $V_{in} = 3.7\,\mathrm{V}$, $C_1 = C_2 = C_3 = 1\,\mu F$, $T = 1\,\mu s$ and the on-resistance of the power-switch $R_{on} = 0.4\,\Omega$.

Figure 6 shows the power efficiency of the proposed converter as a function of the parameter D. The theoretical results in Fig.6 were obtained by Eqs.(10), (13), (21), (24), (30), and (33), where $R_{cnt} = R_{on} = 0.4\,\Omega$ and $R_L = 30\,\Omega$. In the case of 1.5 $\times$, 2 $\times$, and 1 $\times$ mode, the converter can achieve the best efficiency by setting the duty factor to 0.46, 0.55, and 0.55, respectively. As Fig.6 shows, the results of the theoretical analyses agree well with the simulated results.

Figure 7 shows the output voltage V_{out} with different conversion ratios. As Fig.7 shows, the proposed converter can realize a 2 $\times$/ 1.5 $\times$/ 1 $\times$ mode of operation, and the theoretical results and the simulated results correspond well in the steady state. The theoretical results in Fig.7 were obtained by Eqs.(10), (12), (21), (23), (30), and (32), where $R_{cnt} = R_{on} = 0.4\,\Omega$ and $R_L = 30\,\Omega$.

Figure 8 shows the power efficiency of the proposed converter as a function of the output load R_L. In the case of the 1.5 $\times$ mode, the power efficiency is 92.8 % in the output current about $250\,\mathrm{mA}$. Of course, the power efficiency of the proposed converter can be improved by using the power-switches with small on-resistance. As Fig.8 shows, the theoretical results obtained by Eqs.(10), (13), (21), (24), (30), and (33) agree well with the simulated results.

Figure 9 shows the comparison of the power efficiency between the proposed converter and the conventional converter as a function of the output voltage V_{out}. In Fig.9, the regulation of the output voltage was achieved by using an on-resistance control scheme [9,12,13,16]. As Fig.9 shows, the proposed converter can improve the power efficiency in the range of the 1.5 $\times$ mode.

5. Conclusion

For mobile applications, an SC DC-DC converter which offers a 2 $\times$/ 1.5 $\times$/ 1 $\times$ mode of operation has been proposed in this paper. The validity of the circuit design was confirmed by theoretical analyses

and SPICE simulations.

Concerning the power efficiency and the optimal duty factor, the derived theoretical formulas will be helpful to estimate the circuit characteristics, because the theoretical results and the simulation results corresponded well. Furthermore, the SPICE simulations showed that the proposed converter can realize a 2 $\times$/ 1.5 $\times$/ 1 $\times$ mode of operation. Under the conditions that the input voltage V_{in} =3.7 V, the output load $R_L = 30\,\Omega$, and the output voltage $V_{out} = 3.3 \sim 5.3$ V, the proposed converter can improve the power efficiency more than twice from that of the conventional circuit.

The further improvement of efficiency is left to the future study.

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References

[1] I.Harada, F.Ueno, T.Inoue, and I.Oota, "Characteristics analysis of Fibonacci type SC transformer," *T.IEICE, Fundamentals*, Vol.E75-A, No.6, pp.655-662, 1992.

[2] T.Tanzawa and T.Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *T.IEEE, Solid-State Circuits*, Vol.32, No.8, pp.1237-1240, 1997.

[3] N.Hara, I.Oota, F.Ueno, and T.Inoue, "A new ring type set-up switched-capacitor DC-DC converter with low inrush current at start-up and low current ripple in steady state," *T. IEEJ*, Vol.J81-CII, No.7, pp.600-612, 1998.

[4] N.Hara, I.Oota, I.Harada, and F.Ueno, "Programmable ring type switched-capacitor DC-DC converters," *T. IEEJ*, Vol.J82-C-II, No.2, pp.56-68, 1999.

[5] S.H.Chung, "Design and analysis of a switched-capacitor-based step-up DC/DC converter with continuous input current," *IEEE Trans. Circuits Systs.I*, Vol.46, No.6, pp.722-730, 1999.

[6] T.Myono, A.Uemoto, S.Kawai, E.Nishibe, S.Kikuchi, T.Iijima, and H.Kobayashi, "High-efficiency charge-pump circuits with large current output for mobile equipment applications," *T.IEICE, Electron.*, Vol.E84-C, No.10, pp.1602-1611, 2001.

[7] K.Min and J.Ahn, "CMOS charge pumps using cross-coupled charge transfer switches with improved voltage pumping gain and low gate-oxide stress for low-voltage memory circuits," *T. IEICE, Electron.*, Vol.E85-C, No.1, pp.225-229, 2002.

[8] K.Yamada, N.Fujii, and S.Takagi, "Capacitance value free switched capacitor DC-DC voltage converter realizing arbitrary rational conversion ratio," *T. IEICE, Fundamentals*, Vol.E87-A, No.2, pp.344-349, 2004.

[9] K.Eguchi, F.Ueno, H.Zhu, T.Tabata, and T.Inoue, "Design of a charge-average type SC DC-DC converter for cellular phone," *T. IEEJ*, Vol.125-C, No.1, pp.37-42, 2005.

[10] S.V.Cheong, S.H.Chung, and A.Ioinovici, "Inductorless dc-to-dc converter with high power density," *IEEE Trans. Ind. Electron.*, Vol.41, pp.208-215, 1994.

[11] O.C.Mak, Y.C.Wong, and A.Ioinovici, "Step-up dc power supply based on a switched-capacitor circuit," *IEEE Trans. Ind. Electron.*, Vol.42, pp.90-97, 1995.

[12] F.Ueno, T.Inoue, T.Umeno, and I.Oota, "Analysis and application of switched-capacitor transformers by formulation," *Electron. Commun. Japan Pt.II — Electron.*, Vol.73, No.9, pp.91-103, 1990.

[13] S.H.Chung, S.Y.Hui, and S.C.Tang, "Development of a multistage current-controlled switched-capacitor step-down DC/DC converter with continuous input current," *IEEE Trans. Circuits Systs.I*, Vol.47, No.7, pp.1017-1025, 2000.

[14] P.Favrat, P.Deval, M.J.Declercq, "A high-efficiency CMOS voltage doubler," *IEEE journal of Solid-State Circuits*, Vol.33, No.3, pp.410-416, 1998.

[15] D.Maksimovic, S.Dhar, "Switched-capacitor DC-DC converters for low-power on-chip applications," *Proc. of IEEE PESC'1999*, Vol.1, pp.54-59, 1999.

[16] B.R.Gregoire, "A compact switched-capacitor regulated charge pump power supply," *IEEE J.Solid-State Circuits*, Vol.41, No.8, pp.1944-1953, 2006.

6. Appendix

In this section, the properties of the voltage doubler circuit are analyzed.

Figure 10 shows the conventional converter [4] proposed in [14,16]. In Fig.10, the switches S_1 and S_2 are driven by non-overlapped 2-phase clock pulses.

Figure 11 shows the instantaneous equivalent circuits of the converter. In the case of $State - T1$, the capacitor C_1 is charged by the input voltage V_{in} via S_1's. Therefore, the voltage of C_1 becomes V_{in}. In this timing, the output voltage is provided by C_2. On

[4] The SC voltage converter LM2681 produced by National Semiconductor Corporation has the same structure.

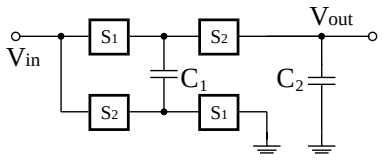
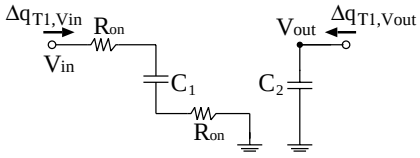
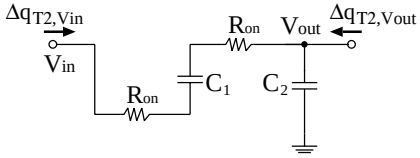


Figure 10. Conventional converter.



(a) $State - T1$ ($S_1 = On$ and $S_2 = Off$)



(b) $State - T2$ ($S_1 = Off$ and $S_2 = On$)

Figure 11. Instantaneous equivalent circuits of Fig.10.

the other hand, in the case of $State - T2$, the input voltage V_{in} and the capacitor C_1 are connected in series via S_2's. Therefore, a stepped-up voltage $2V_{in}$ is obtained in the output terminal under no load condition. The properties of the conventional converter can be obtained as follows:

In the steady state, the differential values of the electric charges in C_1 $(k = 1, 2)$ satisfy

$$\Delta q_{T1}^k + \Delta q_{T2}^k = 0. \quad (34)$$

In the case of $State - T1$, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$ are given by

$$\begin{aligned} \Delta q_{T1,V_{in}} &= \Delta q_{T1}^1 \\ \text{and} \quad \Delta q_{T1,V_{out}} &= \Delta q_{T1}^2. \end{aligned} \quad (35)$$

On the other hand, in the case of $State - T2$, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$ are given by

$$\begin{aligned} &\Delta q_{T2,V_{in}} = -\Delta q_{T2}^1 \\ \text{and} \quad &\Delta q_{T2,V_{out}} = \Delta q_{T2}^1 + \Delta q_{T2}^2. \end{aligned} \quad (36)$$

From Eqs.(34) $\sim$ (36), the average currents of the input and the output are given by

$$\begin{aligned} \overline{I_{in}} &= (\Delta q_{T1,V_{in}} + \Delta q_{T2,V_{in}})/T \\ &= 2\Delta q_{T1}^1/T \\ \text{and} \quad \overline{I_{out}} &= (\Delta q_{T1,V_{out}} + \Delta q_{T2,V_{out}})/T \\ &= -\Delta q_{T1}^1/T. \end{aligned} \quad (37)$$

Therefore, the following equation is derived:

$$\overline{I_{in}} = -2\overline{I_{out}}. \quad (38)$$

In Fig.11, the energy consumed by resistors in one period, W_T, can be expressed by

$$W_T = W_{T1} + W_{T2}, \quad (39)$$

where

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{T1}(\Delta q_{T1}^1)^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{T2}(\Delta q_{T2}^1)^2. \end{aligned}$$

From Eqs.(34) $\sim$ (37), Eq.(39) can be rewritten as

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{DT}(\Delta q_{V_{out}})^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{(1-D)T}(\Delta q_{V_{out}})^2. \end{aligned} \quad (40)$$

By substituting Eq.(40) into Eq.(39), the SC resistance of the doubler circuit, R_{SCC}, can be obtained by

$$R_{SCC} = \frac{2}{D(1-D)} \cdot R_{on}. \quad (41)$$

In Eq.(41), the optimal duty factor is $D = 0.5$. From Eqs.(38) and (41), the equivalent circuit of the conventional converter is expressed by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 2 & 0 \\ 0 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} 1 & R_{SCC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \quad (42)$$

From Eq.(42), the power efficiency η_C of the conventional converter can be given by

$$\begin{aligned} \eta_C &= \frac{R_L \overline{I_{out}}^2}{R_L \overline{I_{out}}^2 + R_{SCC}\overline{I_{out}}^2} \\ &= \frac{R_L}{R_L + R_{SCC}}. \end{aligned} \quad (43)$$

From Eqs.(25) and (41), in the case of the 2 $\times$ mode, the SC resistance of the proposed converter is larger than that of the conventional converter. However, the difference between Eqs.(25) and (41) is only R_{cnt}/D. As Fig.9 shows, the difference between the proposed converter and the conventional converter in the efficiency of the 2 $\times$ mode is very small. Furthermore, in the conventional converter, the power efficiency decreases strongly by the regulation, because the conventional converter cannot achieve a 1.5 $\times$ mode of operation.